IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Petrus Maria De Greef
For	:	DISPLAYING ON A MATRIX DISPLAY
Serial No.	:	10/587,604
Filed	:	July 27, 2006
Art Unit	:	3561
Examiner	:	Edward Martello
Atty. Docket	:	NL040106US1
Confirmation No.	:	3561

APPEAL BRIEF

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Sir:

This Appeal Brief is support of the Notice of Appeal filed March 18, 2009.

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V. by way of an Assignment recorded at Reel 019719, frame 0843.

II. RELATED APPEALS AND INTERFERENCES

Following are identified any prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal:

NONE.

III. STATUS OF CLAIMS

Claims 1-11 are on appeal.

Claims 1-11 are pending.

Claims 1-11 are rejected.

No claims are allowed.

No claims are canceled.

IV. STATUS OF AMENDMENTS

All Amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The subject matter recited in claim 1 relates to a method of displaying an image comprising the steps of: storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants (see Figs. 1 & 2; page 4, lines 18-24), reading

during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate (see page 4, lines 34-39), displaying the display data on a matrix display (see page 3, lines 34-36), and controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate (see Figs. 3 & 5; page 5, lines 9-23).

The subject matter recited in claim 2 relates to a system of displaying an image (see figs. 1 & 2), comprising of: a video source (see page 3, lines 24-28) for generating images comprising source data and source frame synchronization instants having a source frame rate, means (see page 3, lines 18-24) for storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants, means (see page 4, lines 34-39) for reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate, means (see page 3, lines 35-37) for displaying the display data on a matrix display and means (see figs. 3 & 5; page 5, lines 9-23) for controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed

polarity during the read period and a ratio of two between the display frame rate and the source frame rate.

The subject matter recited in claim 5 relates to a system of displaying an image as claimed in claim 4, wherein the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data (see figs. 3 & 5; page 2, lines 53-56).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

A. Claims 1-4 and 6-8 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by European Patent Application Publication EP 0875882 to Schiefer et al. (hereinafter "Schiefer").

B. Claim 5 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schiefer.

C. Claims 9-11 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schiefer in view of U.S. Patent Application 2003/0164897 to Chen et al. (hereinafter "Chen").

VII. ARGUMENTS

A. Rejection of Claims 1-4 & 6-8 Under 35 U.S.C. § 102(b)

The Final Office Action dated December 26, 2008, rejects claims 1-4 and 6-8 under 35 U.S.C. § 102(b) as allegedly being anticipated by Schiefer. Appellant respectfully traverses this rejection.

The test for anticipation under section 102 is whether each and every element set for in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987); MPEP § 2131. The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d § 1913, 1920 (Fed. Cir. 1989); MPEP § 2131. The elements must also be arranged as required by the claim. *In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

1. Claims 1 & 2

Independent claim 1 recites, in part, "A display method comprising . . . controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate" (emphasis added). Independent claim 2 contains similar recitations.

As described in the specification in paragraph [0009], this subject matter relates to the use of a controller to control both the read and write address pointers

in the memory in order to prevent video tearing. If the source and display frame rates are not equal, the controller adjusts both the frame rates and the address pointers so that, during the read period, one pointer does not cross the other, thus preventing tearing. *See* ¶ [0015]. This is highlighted by three features: (1) a time offset between the two address pointers, (2) a fixed polarity of the pointers during the read period, and (3) a constant ratio between the display frame rate and the source frame rate (here, the ratio is equal to 2). *See* ¶ [0054].

In contrast, Schiefer fails to disclose, teach, or suggest "controlling means for controlling the source frame rate or the display frame rate to obtain the address pointers, where the pointers start with a time offset, there is a fixed polarity between the pointers, and there is a ratio of two between the display and source frame rates," as recited in claim 1 and similarly recited in claim 2. The Examiner alleges that, because the write counter is initialized at the start of the frame and is used as a pointer with the reading delayed until the buffer is half full, Schiefer reads on the claims as written.

Appellant respectfully disagrees with this assertion. Schiefer discloses a timing generator for format conversion of video. *See* Abstract. This system reformats video by synchronizing the output and input rates and using a memory buffer to ensure smooth display. The memory write controller controls write operations sequentially in a circular buffer sequence. *See* col. 13, ln. 34-39. The data path, once full, is then controlled by a timing controller.

The display synchronizer uses vertical and horizontal synchronization signals to force synchronization between the display timing generator and the video input signal. *See* col. 17, ln. 53-57. The system supports multiple synchronization modes. *See* col. 18, ln. 7-10. Of greatest interest are the line synchronization and frame synchronization modes. *See* col. 20, ln. 23 – col. 21, ln. 46. In "Line Synch" mode, the display line rate is a function of the input video main clock. *See* col. 21, ln. 15-20. In "Frame Synch" mode, the input signal is locked to the output signal on a frame-by-frame basis. *See* col. 21, ln. 34-36.

However, Schiefer discloses a half-line offset usually used in interlacing in order *to maintain a constant period*. *See* col. 17, ln. 12-20. The Schiefer application does not discuss the polarity of the pointers, nor does Schiefer disclose using a fixed ratio between frame rates, as Schiefer's synchronization modes either synchronize frames based on a clock or synchronize frames so that they each have the substantially the same frame rate. This rate as disclosed in Schiefer is much closer than the 2:1 ratio of frame rates recited in independent claims 1-2.

As such, Schiefer fails to read on all the elements recited in claims 1 and 2, as the invention disclosed by Schiefer would not function in the range of frame rates as recited in claims 1 and 2. *See* MPEP § 2131.03. Therefore, Appellant believes that the Examiner erred in rejecting independent claims 1 and 2 under 35 U.S.C. § 102(b) as allegedly being anticipated by Schiefer.

2. Claims 3, 4, and 6-8

Claims 3, 4, and 6-8 depend on claim 2 and are therefore also patentable for at least the reasons stated above in connection with claim 1, as well as for the separately patentable subject matter recited therein.

B. Rejection of Claim 5 Under 35 U.S.C. § 103(a)

The Final Office Action dated December 26, 2008, rejects claim 5 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schiefer. Appellant respectfully traverses this rejection.

The United States does not grant patents for inventions that would have been obvious to a person of ordinary skill in the art at the time of the invention. 35 U.S.C. § 103 (2000); MPEP § 2142. In an obviousness inquiry, the court first determines 1) the scope and content of the prior art; 2) the differences between the claimed invention and the prior art; 3) the level of ordinary skill in the art; and 4) secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 1718 (1966).

Dependent claim 5 recites, in part, "[a] display system as claimed in claim 4, wherein the means for adapting are arranged to obtain an offset in time between the first pointer and the second pointer being substantially equal to half a source write period . . ."

As described in the specification in paragraph [0054], this subject matter relates to the time between the address pointers. In this instance, the time offset is the maximum distance between the pointers, as illustrated in Figs. 3 & 5C. As the

two address pointers have the same polarity, the pointers have a minimum probability of crossing each other. This allows for a large difference in frame rates (where one frame rate is substantially equal to twice the frame rate of the other) between the source and display, while still avoiding video tearing.

In contrast, Schiefer fails to disclose, teach or suggest ". . . an offset in time between the first pointer and the second pointer being substantially equal to half a source write period," as recited in claim 5. The Examiner alleges that, in view of Schiefer, it would have been obvious to maintain an average amount of data in the buffer to equally prevent an underflow or overwrite condition, which would be approximately half the buffer memory size.

Apellant disagrees with this assertion. A person of ordinary skill in the art would not have modified the invention of Schiefer to operate in the manner recited in claim 5. An invention that otherwise might be viewed as an obvious modification of prior art will not be deemed obvious when a prior art reference teaches away from the invention. *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1354 (Fed. Cir. 2000).

In the instant case, Schiefer discloses the use of half-line offset "to maintain a constant period between lock events" with regard to the source and output having substantially the same frame rates, where the choice of offset time is used to minimize timing errors. Col. 17, ln. 17-20. A person of ordinary skill in the art would not modify Schiefer to achieve the subject matter recited in claim 5, however, as Schiefer discloses such use when the input and output have the same frame rate.

Instead, given a substantial difference in frame rates as recited in claim 5, a person of ordinary skill in the art applying the teachings of Schiefer would choose a point between the two frame rates that would give equal protection between overwrite and underflow conditions. Such a solution would be substantially different from the half-line offset recited in claim 5. As Schiefer would teach a person of ordinary skill in the art away from the subject matter recited in claim 5, Schiefer does not render claim 5 obvious.

Claim 5 also depends from claim 4, which depends from claim 2, and is therefore also patentable for at least the reasons stated above in connection with claim 2, as well as for the separately patentable subject matter recited therein.

C. Rejection of Claims 9-11 Under 35 U.S.C. § 103(a)

The Final Office Action dated December 26, 2008, rejects claims 9-11 under 35 U.S.C. § 103(a) as being unpatentable over Schiefer in view of Chen. Appellant respectfully traverses this rejection.

Claims 9-11 depend on claim 2. Chen discloses a system to prevent buffer over/under-flow, with the input and output rate matching. *See* Abstract. Chen also discloses a display frame period being the inverse of the display frame rate and controlling the display frame rate by adjusting the idle time (time between read periods). Chen therefore fails to overcome the deficiencies of Schiefer described above in connection with the rejection of independent claim 2. Claims 9-11 are

therefore patentable for at least the reasons stated above in connection with claim 2, as well as for the separately patentable subject matter recited therein.

D. Conclusion

For at least the reasons discussed above, it is respectfully submitted that the rejections are in error and that claims 1-11 are in condition for allowance. For at least the above reasons, Appellants respectfully request that this Honorable Board reverse the rejections of claims 1-11.

Respectfully submitted,
KRAMER & AMADO, P.C.

March 18, 2009
Date

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VIII. CLAIMS APPENDIX

CLAIMS INVOLVED IN THE APPEAL:

1. (Previously Presented) A display method comprising:

generating images comprising source data and source frame synchronization instants having a source frame rate,

storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants,

reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate,

displaying the display data on a matrix display, and

controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate.

2. (Previously Presented) A display system comprising:

a video source for generating images comprising source data and source frame synchronization instants having a source frame rate,

means for storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants,

means for reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate,

means for displaying the display data on a matrix display and means for controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate.

3. (Previously Presented) A display system as claimed in claim 2, wherein the means for controlling comprise:

means for comparing the source frame synchronization instants and the display synchronization instants or signals related thereto, and

means for adapting the source frame rate or the display frame rate in response to the comparing to obtain the second pointer always lagging the first pointer during the read period in times or the other way around.

4. (Previously Presented) A display system claimed in claim 2, wherein the means for controlling comprise:

means for determining the offset in time between one of the source frame synchronization instants and one of the display frame synchronization instants succeeding each other, and

means for adapting the source frame rate or the display frame rate to obtain a substantially identical source frame rate and display frame rate and a predetermined fixed value of the offset in time.

5. (Previously Presented) A display system as claimed in claim 4, wherein the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data.

6. (Previously Presented) A display system as claimed in claim 2, wherein the means for displaying the display data further comprise:

means for generating a clock signal, and means for generating the display frame synchronization instants using the clock signal, and wherein

the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal.

7. (Previously Presented) A display system as claimed in claim 2, wherein the means for displaying the display data further comprise:

means for generating a clock signal, means for generating line instants indicating a start of the lines of the display data using the clock signal, the line instants determining line periods, and

means for generating the display frame synchronization instants using the line instants, and wherein

the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal to vary a duration of the line periods.

8. (Previously Presented) A display system as claimed in claim 2, wherein the means for displaying the display data further comprise:

means for generating a clock signal, means for generating line instants indicating a start of the lines of the display data by counting the clock signal, the line instants determining line periods, and

means for generating the display frame synchronization instants using the line instants, and wherein

the means for controlling the display frame rate comprise means for adapting a frequency of the clock signal to vary a duration of the line periods.

9. (Previously Presented) A display system method as claimed in claim 2, wherein a display frame period has a duration being an inverse of the display frame rate and comprises the means for the read period and an idle period,

wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer, and

wherein during the idle period no display data is read from the memory and wherein the means for controlling the display frame rate comprises means for varying the idle time.

10. (Previously Presented) A display system as claimed in claim 2, wherein the means for controlling comprise:

means for determining the offset in time, and

means for adapting the display frame rate to obtain a display frame rate being substantially identical to two times the source frame rate and to obtain a predetermined fixed offset in time, by having

(i) the second pointer pointing to a first source video line of an already stored source video frame at an instant preceding the instant the first pointer is pointing to a first source video line a next source video frame to read the first source video line before the first source video line of the next source video frame is stored, and

(ii) the second pointer pointing to a last source video line of the next source video frame at an instant later than an instant the first pointer is pointing to the last source video line of the next source video frame to read the last source video line of the next source video frame after it has been stored.

11. (Previously Presented) A display system as claimed in claim 2, wherein a display frame period has a duration being an inverse of the display frame rate and comprises the read period and an idle period, wherein during the read period, the means for reading are arranged for reading the display data from the memory under control of the second address pointer, and wherein during the idle period no display data is read from memory and wherein the means for controlling comprise:

means for setting a free running display frame rate to a value lower than the value of the source display frame rate wherein a duration of the read period is shorter than a source frame period, and

means for restarting the display frame periods in response to received source synchronization instants.

IX. EVIDENCE APPENDIX

A copy of the following evidence 1) entered by the Examiner, including a statement setting forth where in the record the evidence was entered by the Examiner, 2) relied upon by the Appellant in the appeal, and/or 3) relied upon by the Examiner as to the grounds of rejection to be reviewed on appeal, is attached:

NONE

X. RELATED PROCEEDINGS APPENDIX

Following are identified any prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending appeal:

NONE